

Figure 1
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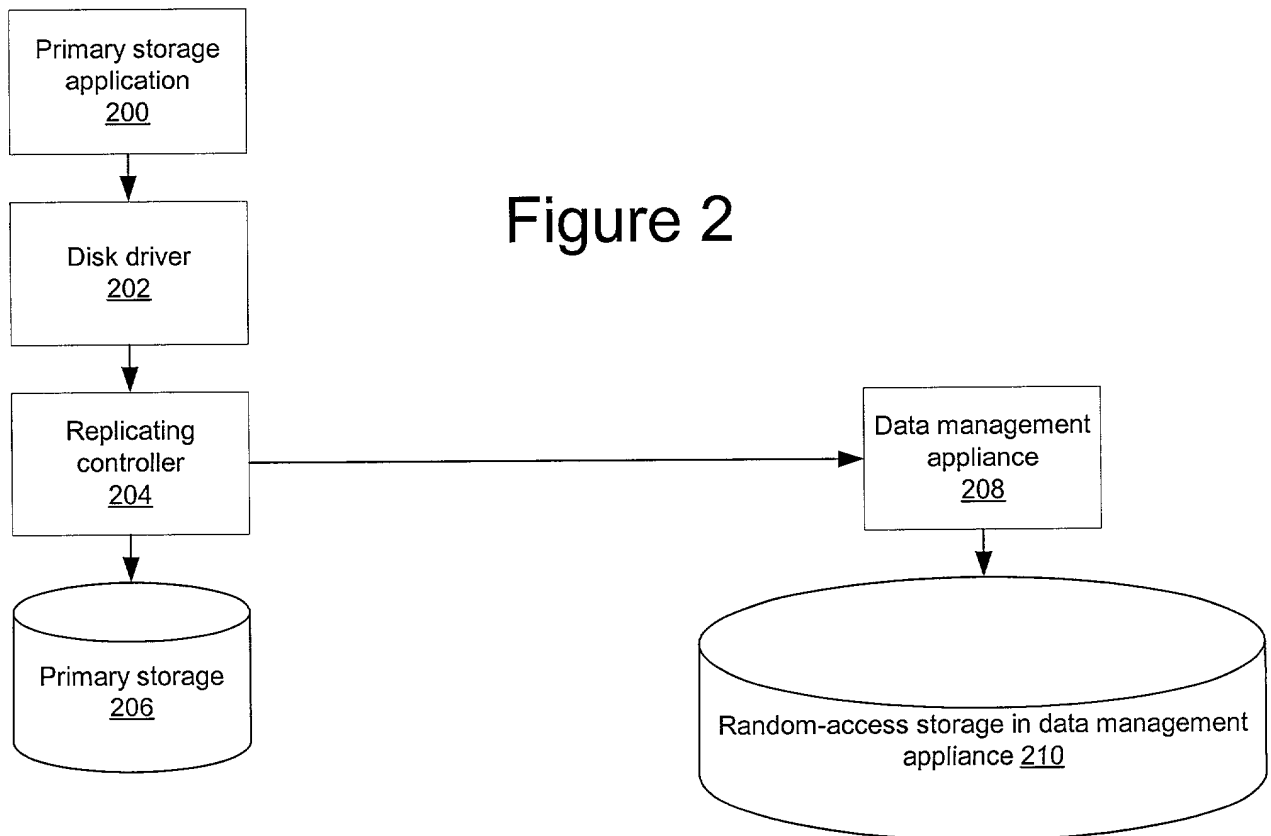


Figure 2

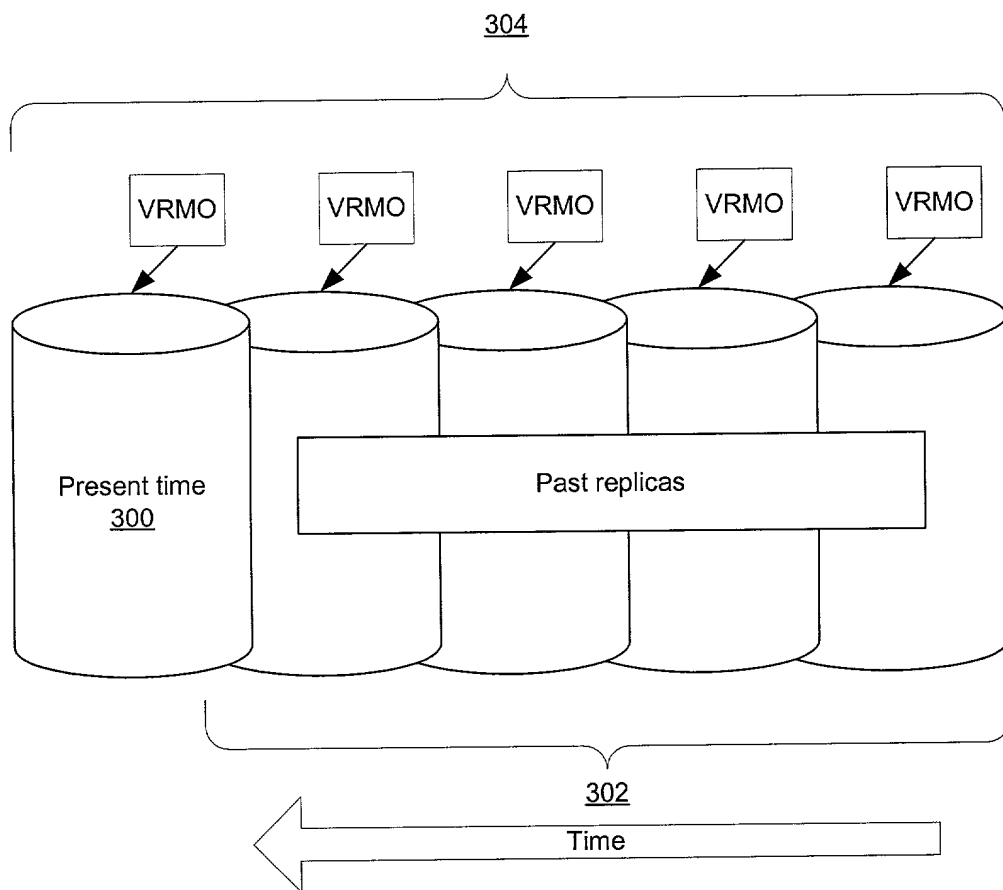


Figure 3

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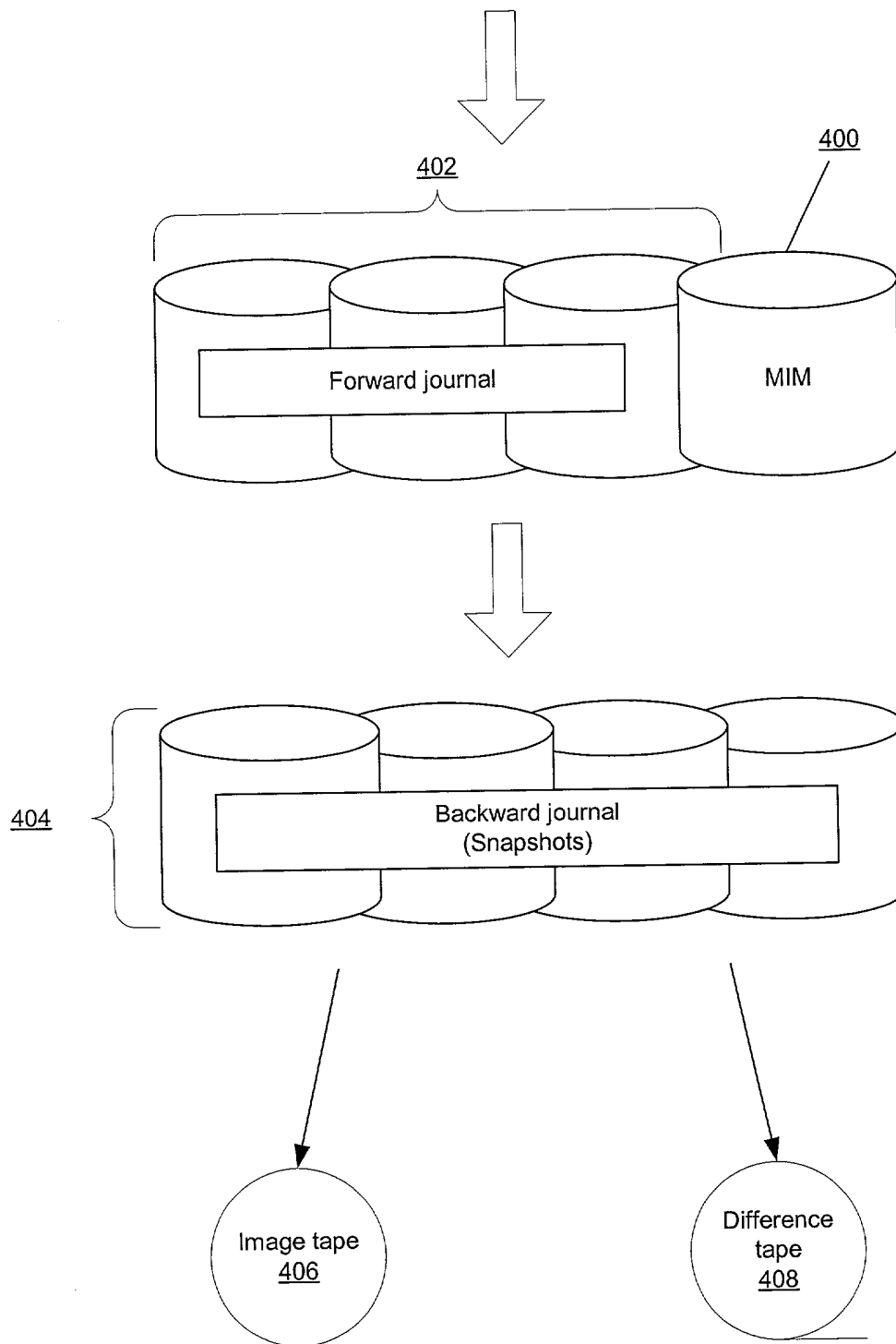


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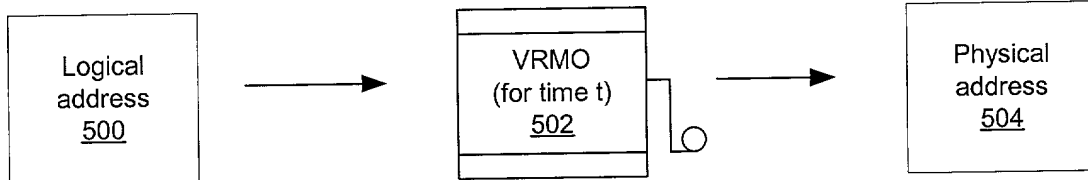
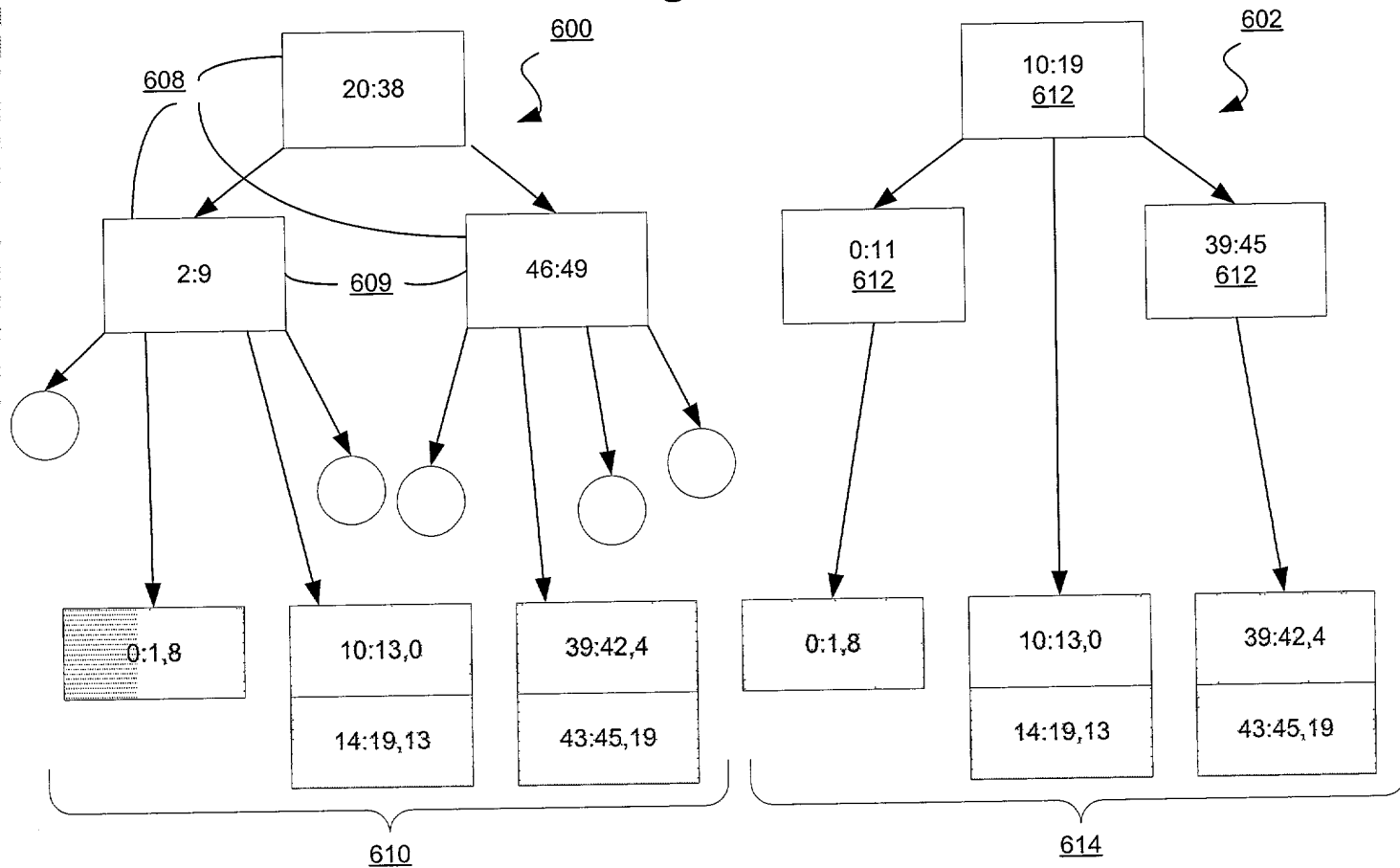


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Figure 6



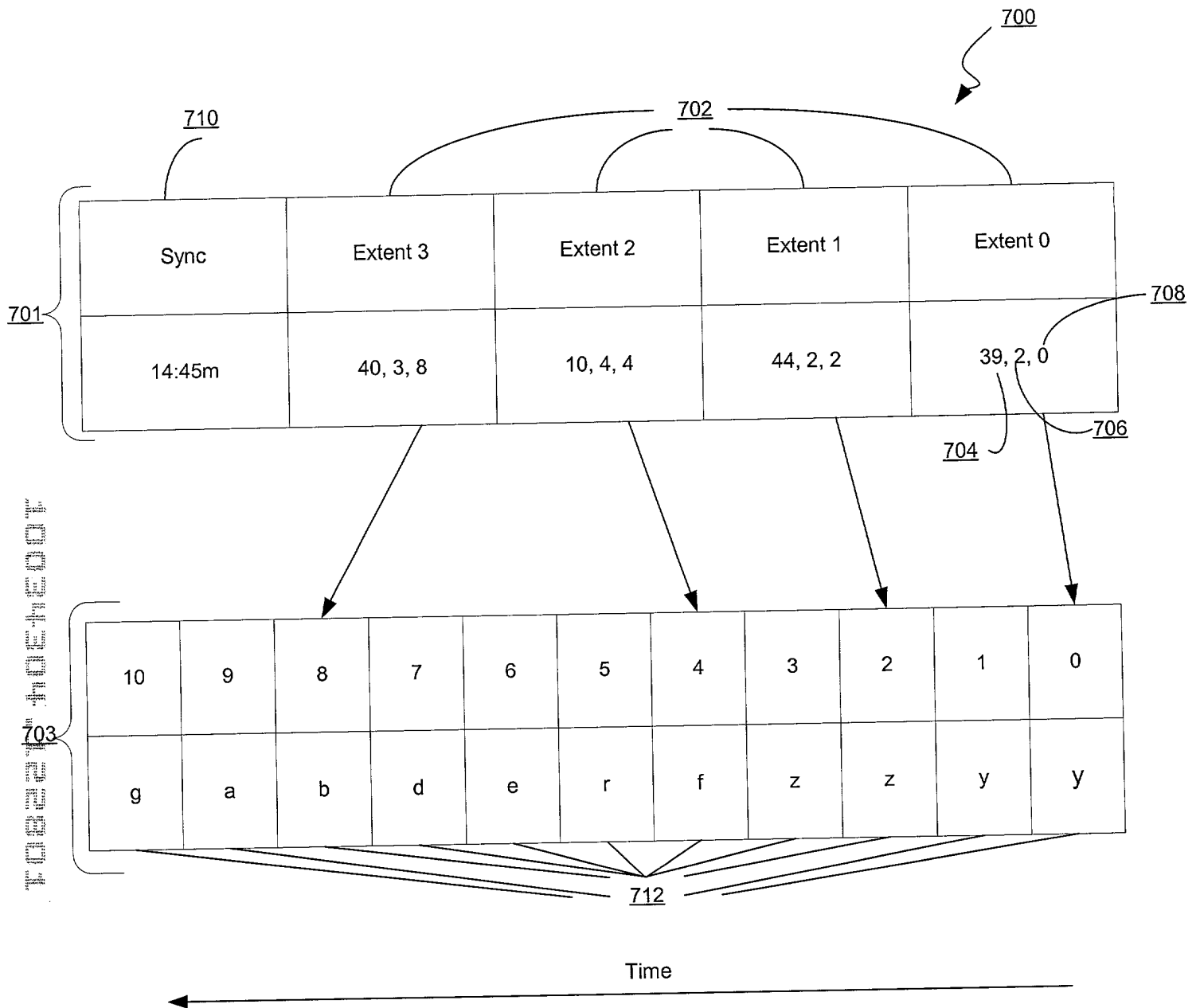


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800

802

804

0	1	2	3	4	5	6	7	8	9
Q	Q	Q	Q	Q	Q	Q	Q	Q	Q
10	11	12	13	14	15	16	17	18	19
R	R	R	R	R	R	R	R	R	R
20	21	22	23	24	25	26	27	28	29
S	S	S	S	S	S	S	S	S	S
30	31	32	33	34	35	36	37	38	39
T	T	T	T	T	T	T	T	T	T
40	41	42	43	44	45	46	47	48	49
U	U	U	U	U	U	U	U	U	U

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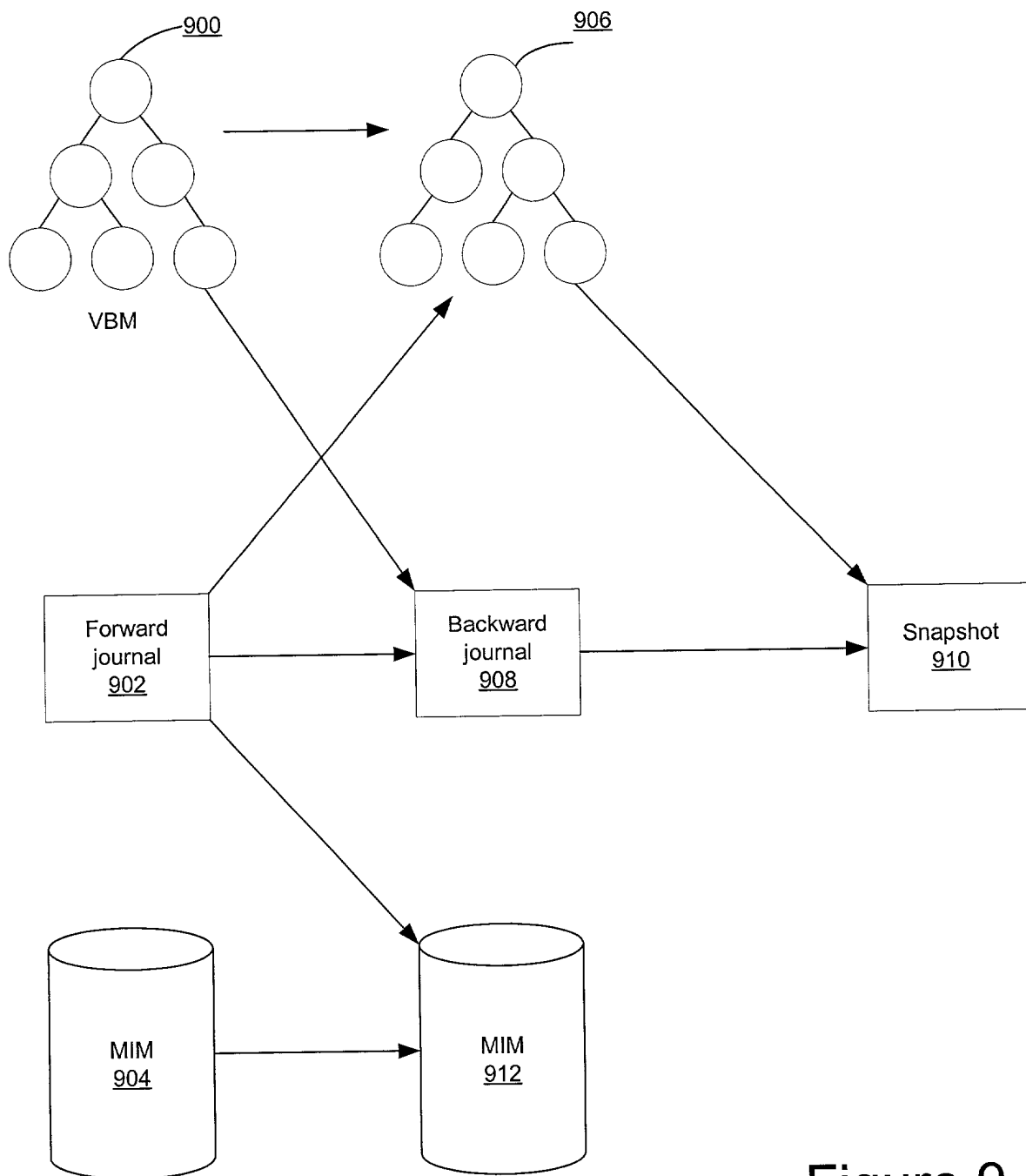


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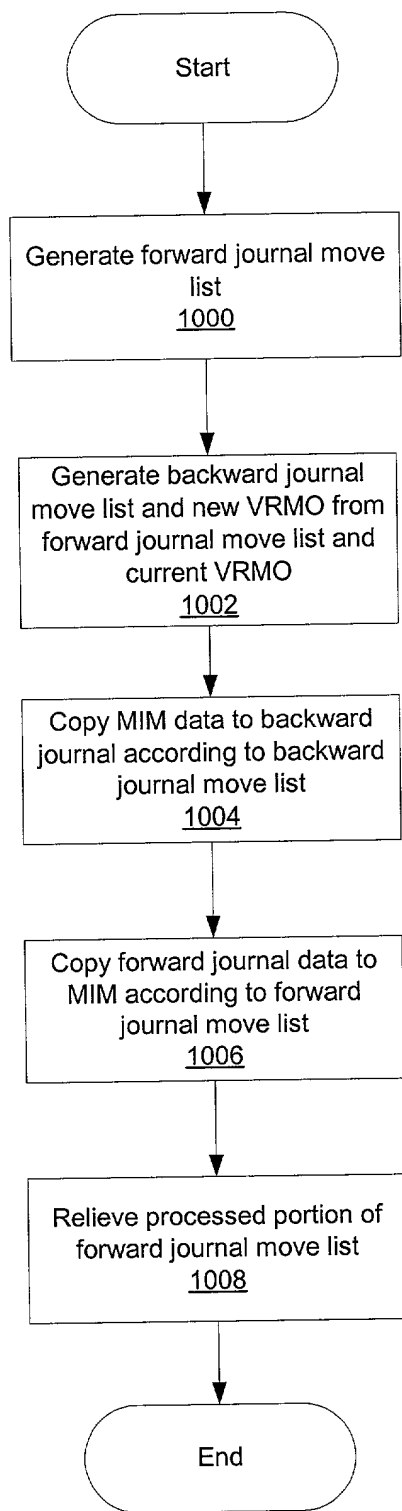


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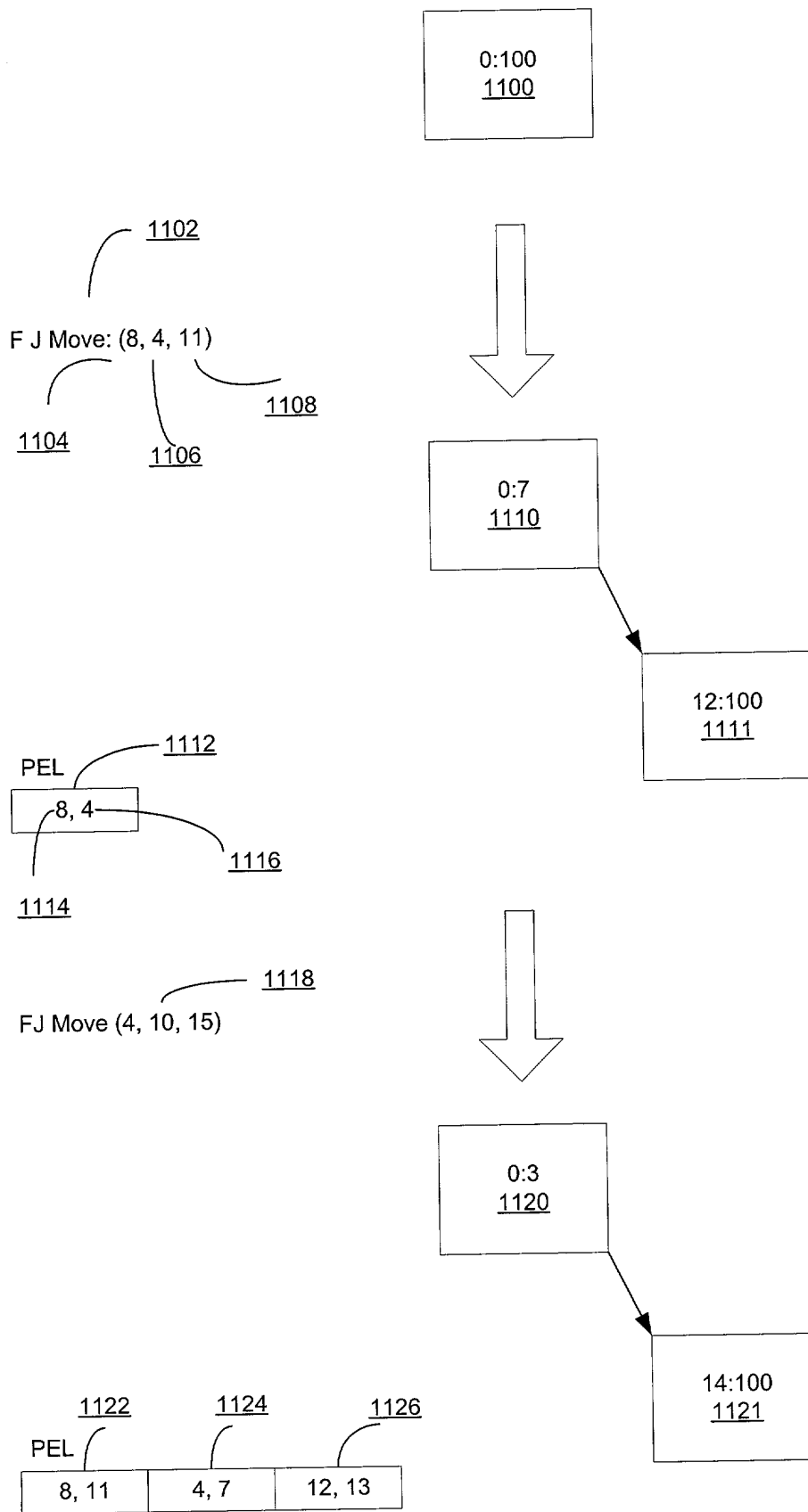


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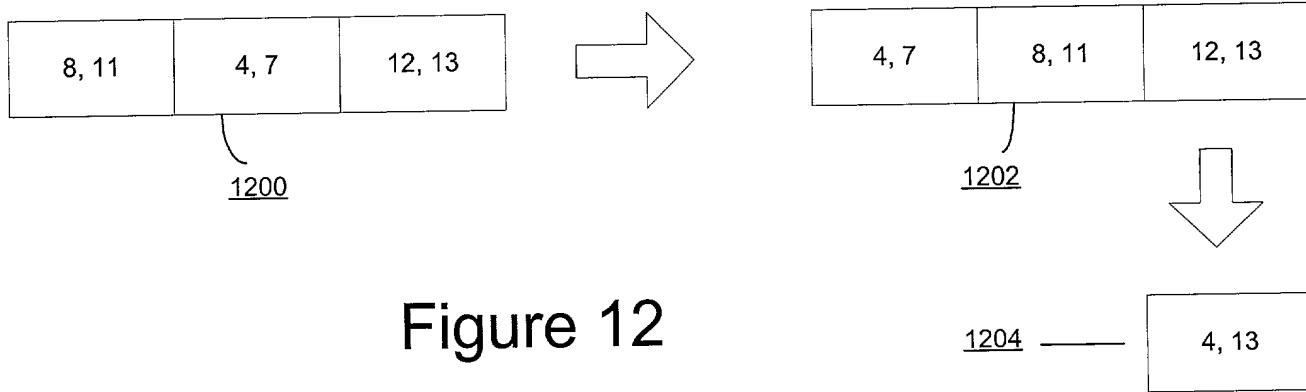


Figure 12

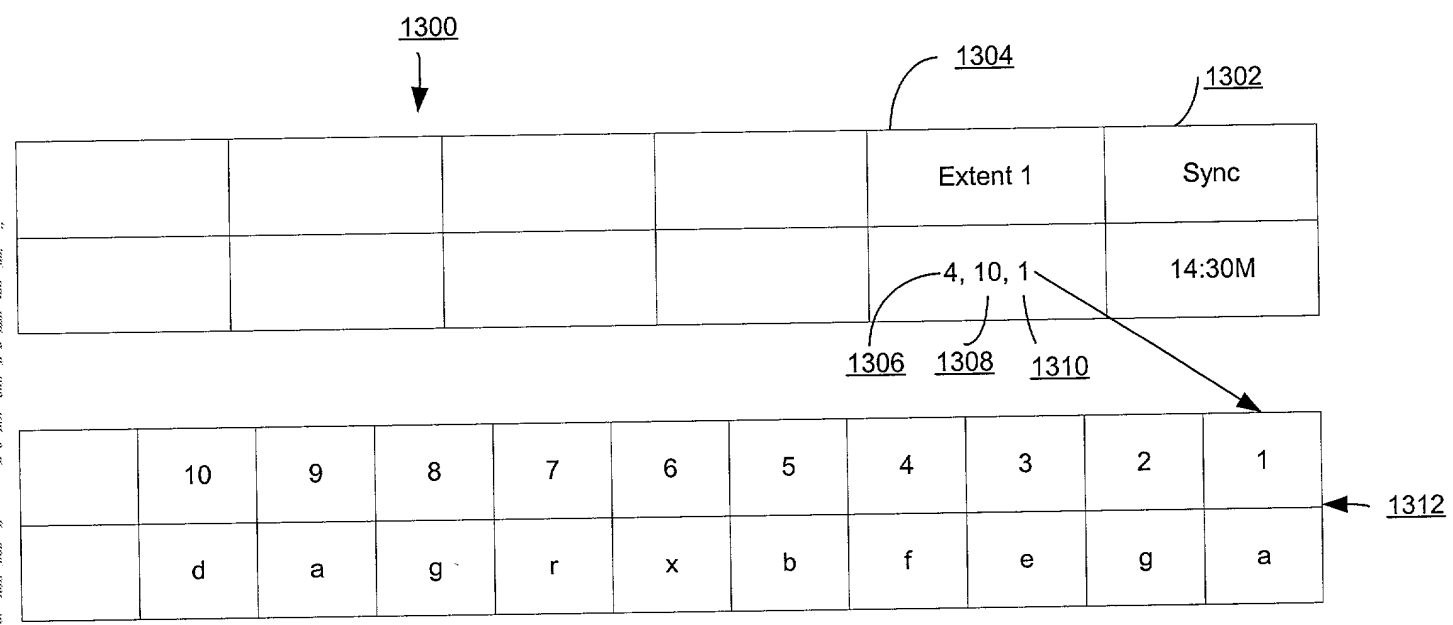


Figure 13

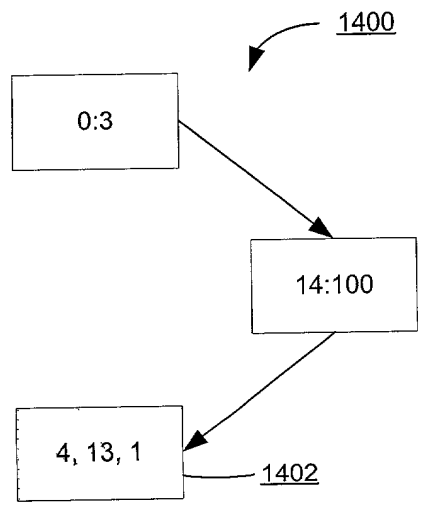


Figure 14

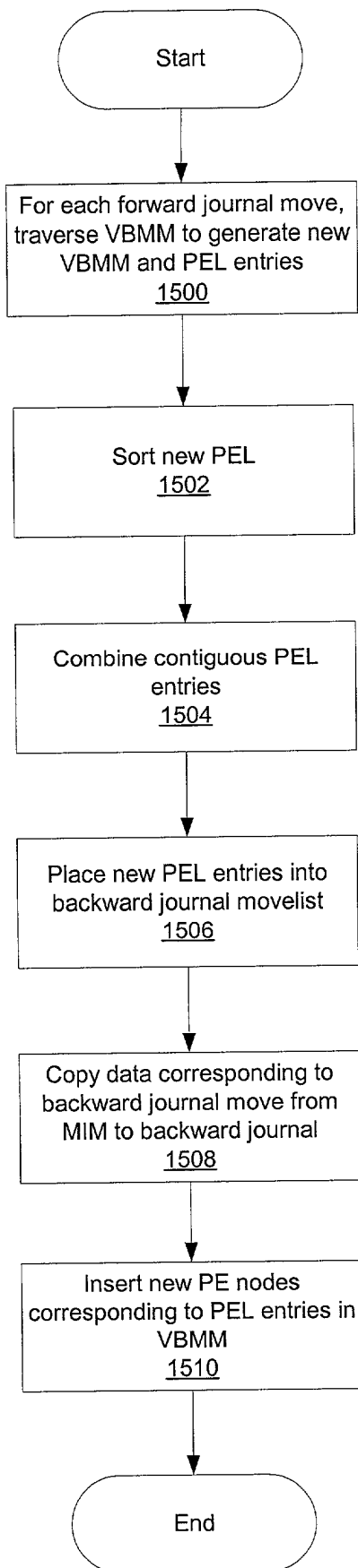


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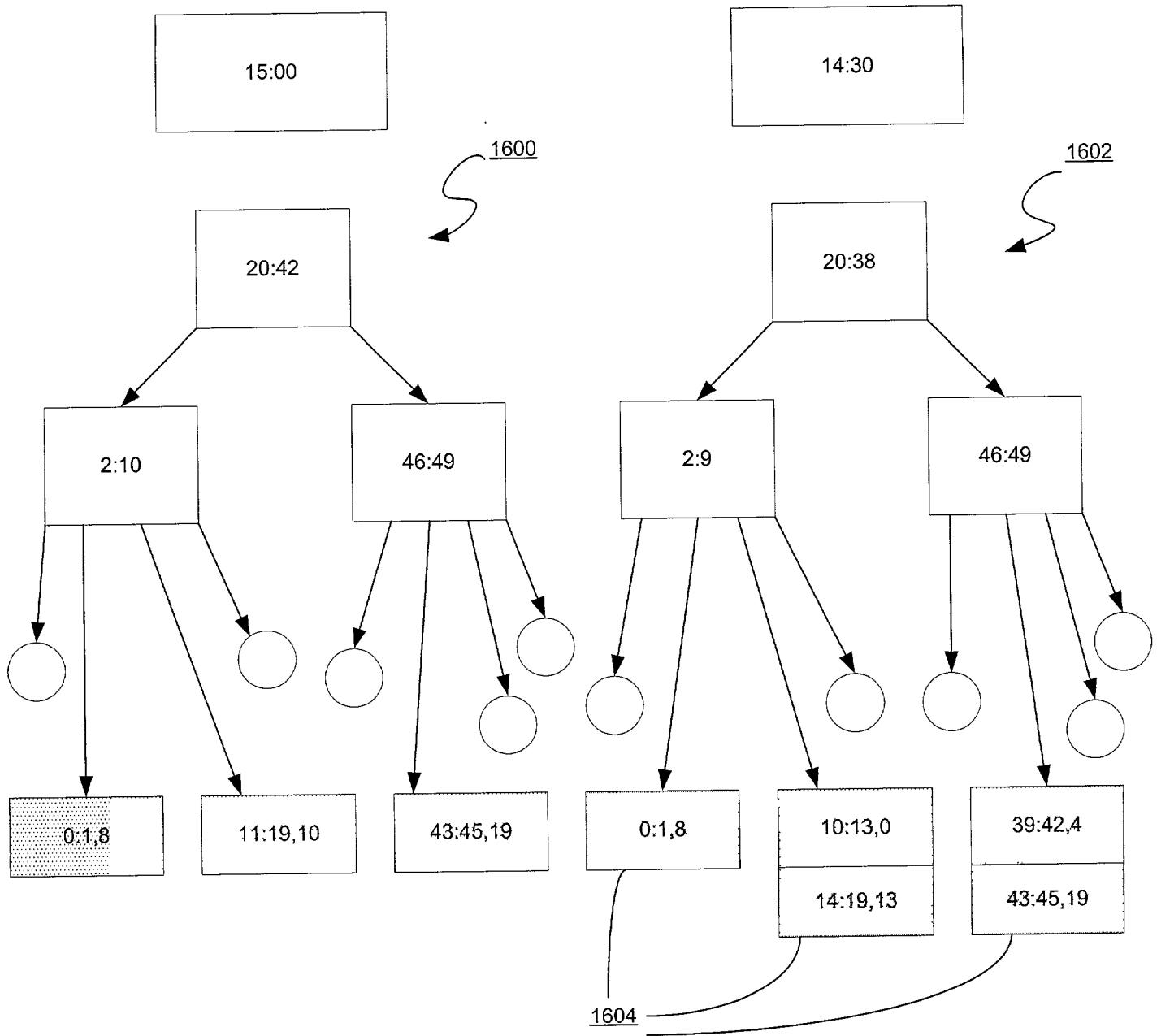


Figure 16

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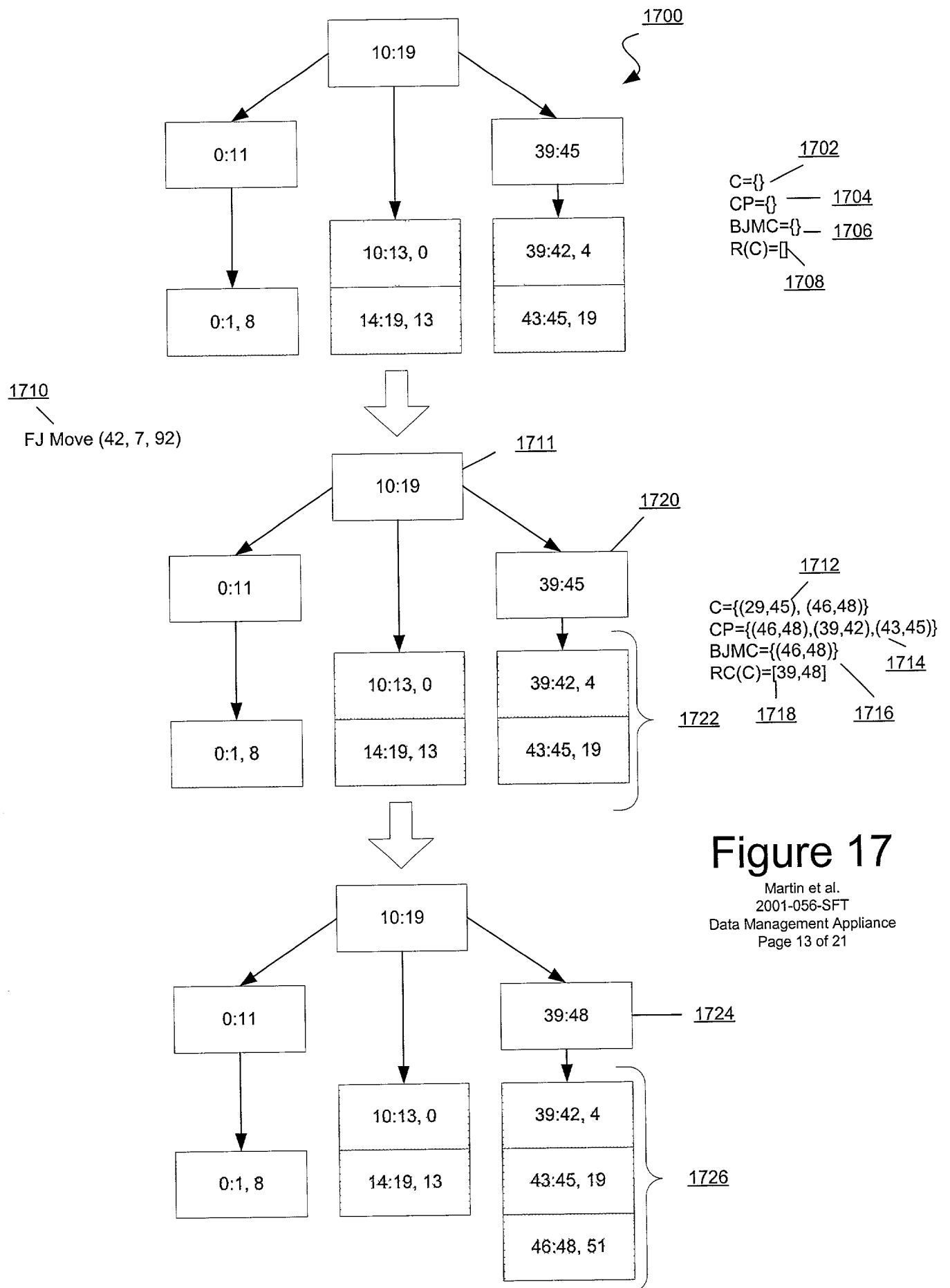


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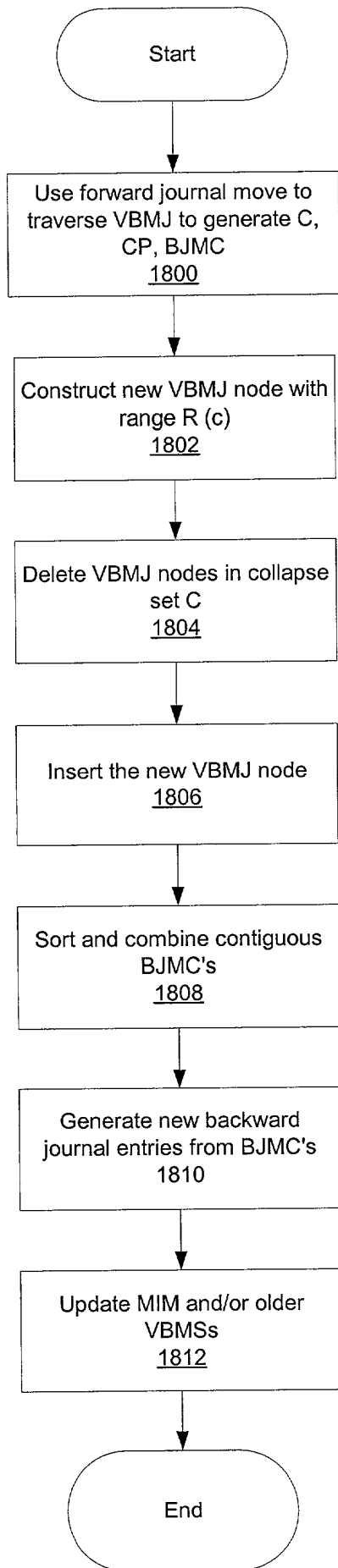


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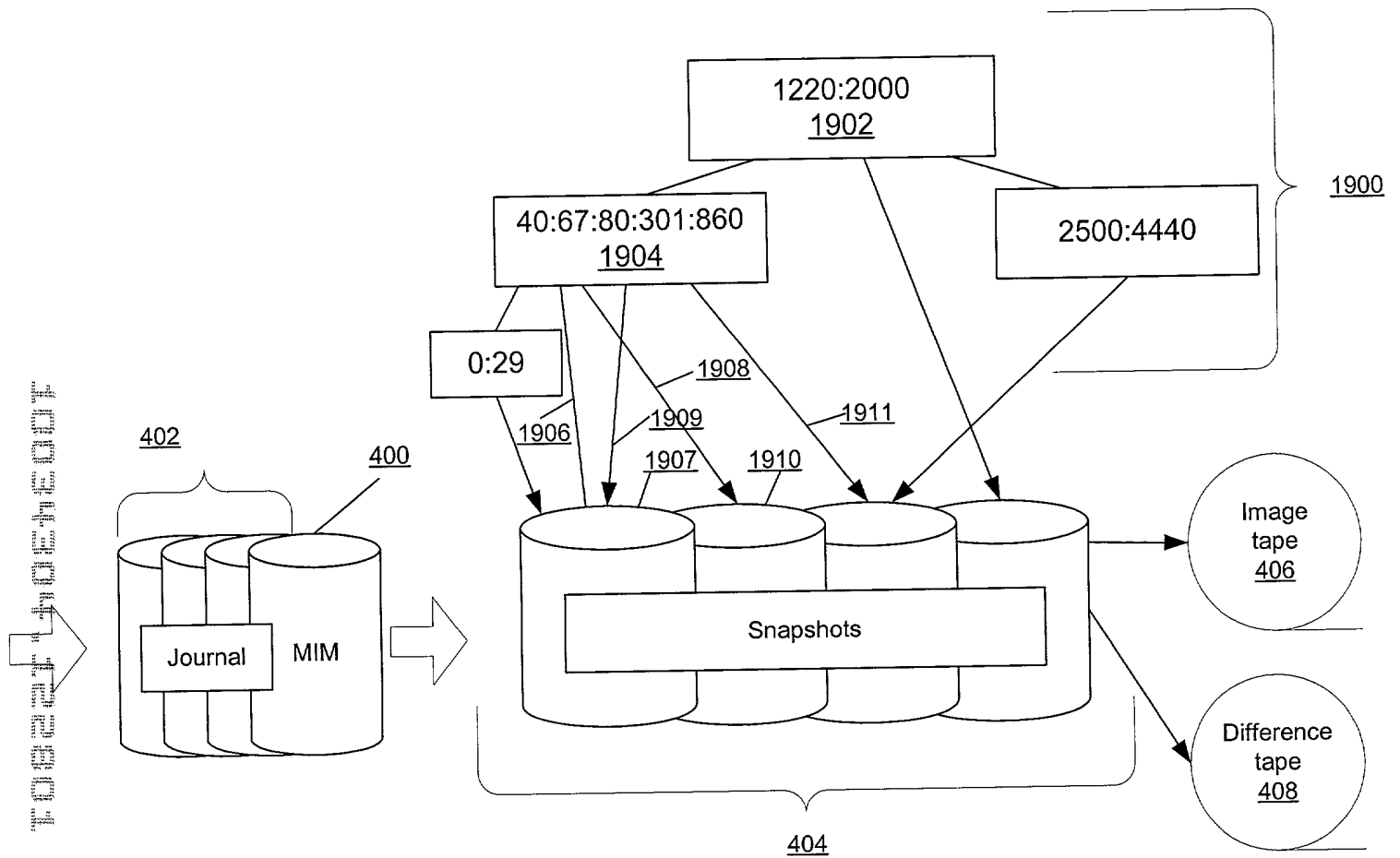


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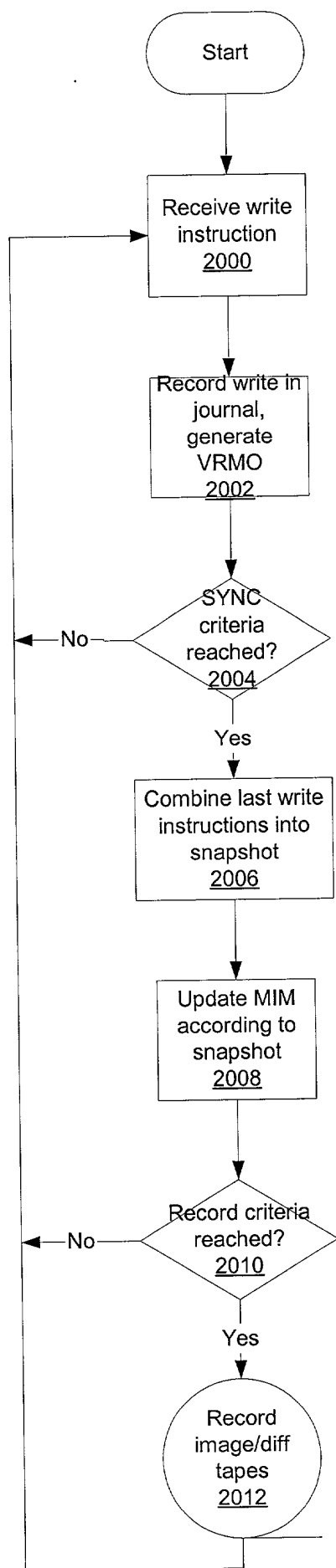


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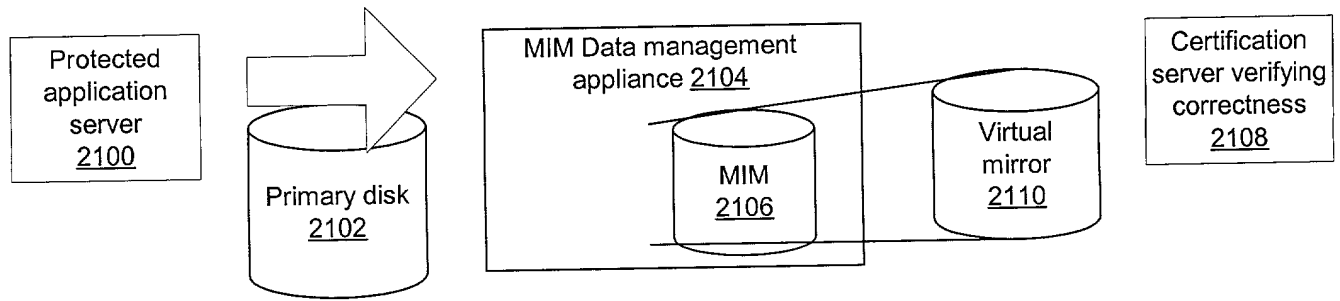


Figure 21

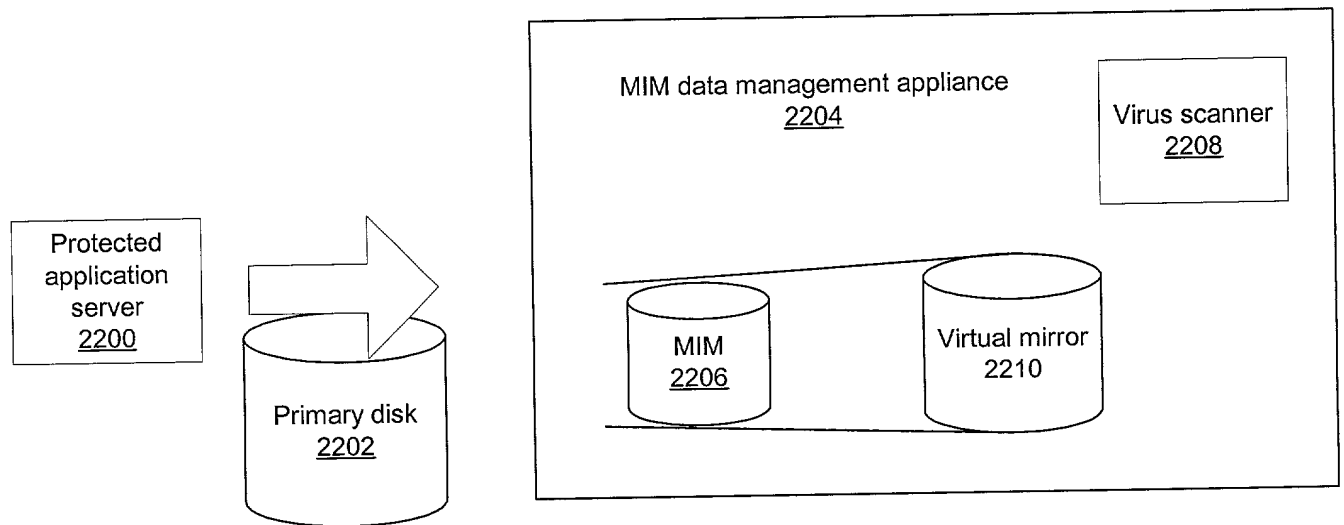


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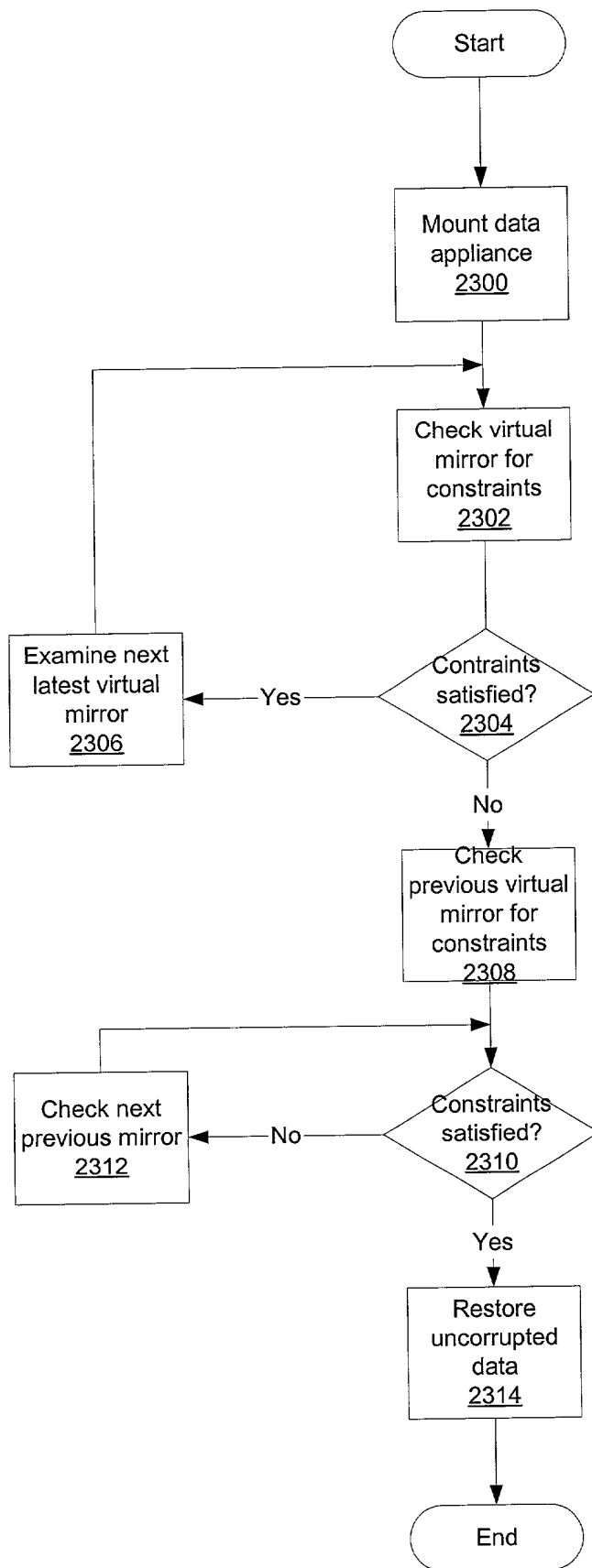


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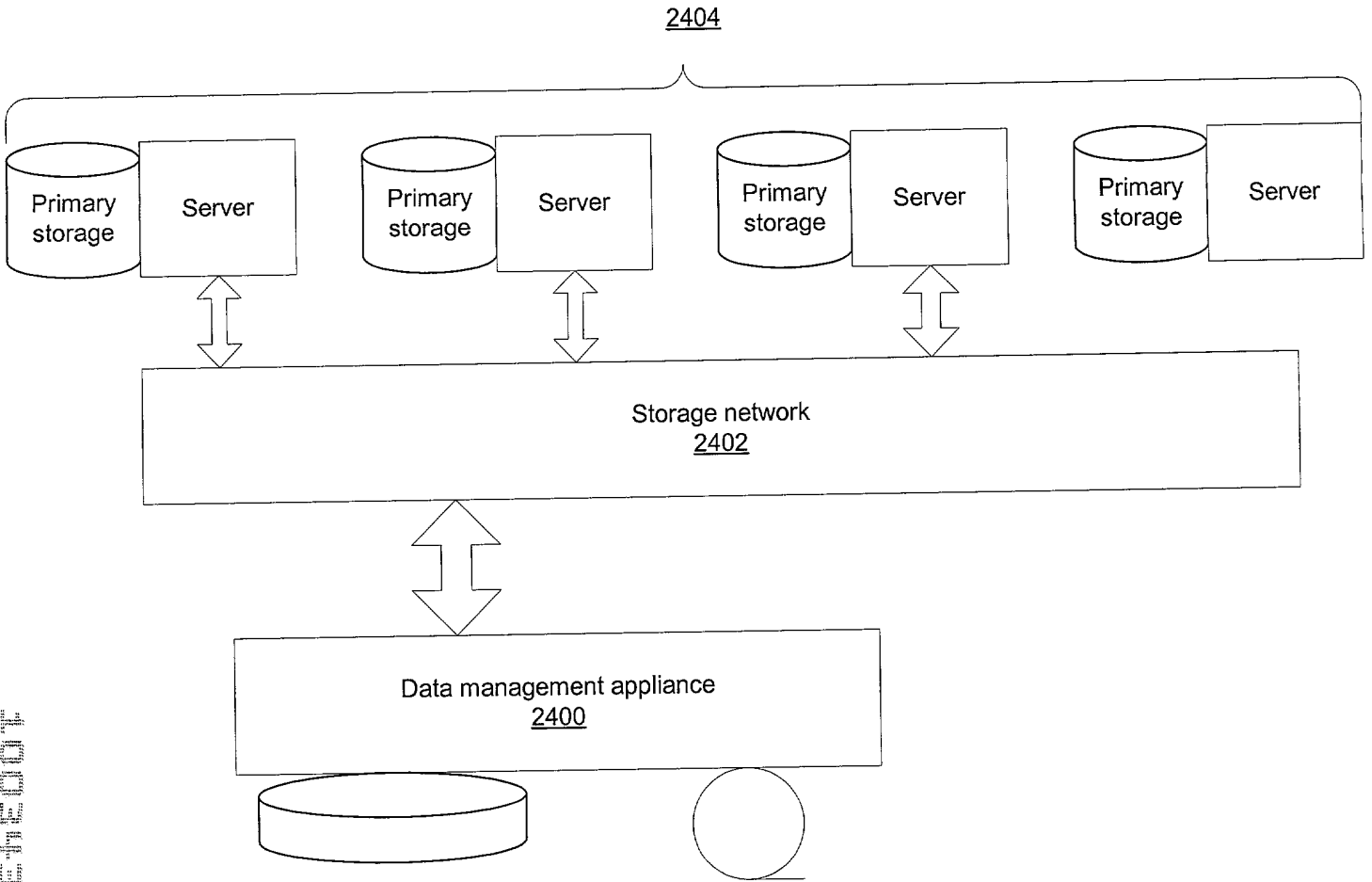
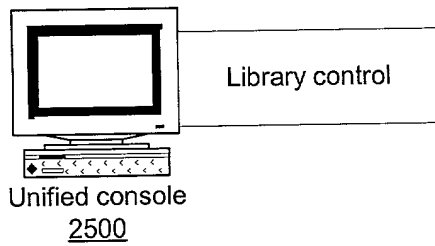
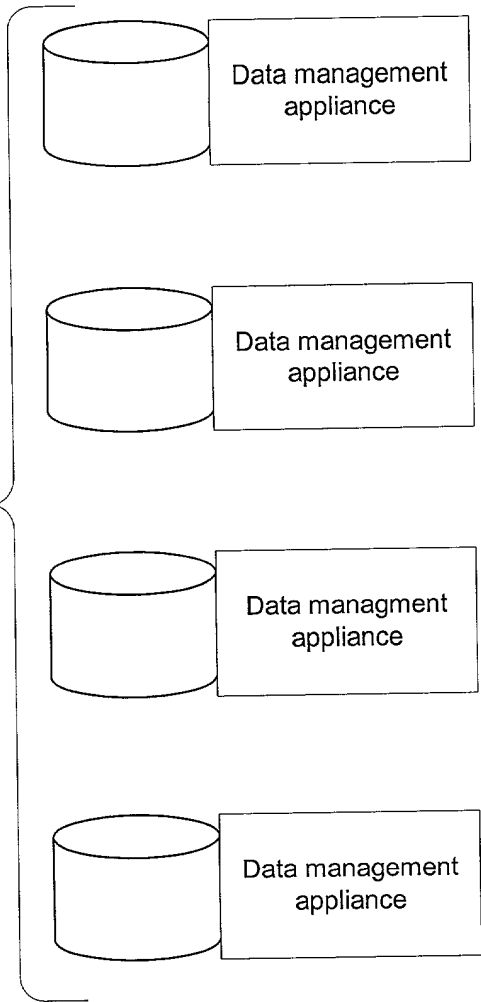


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FIG. 24

2504



SAN switch
2506

2502

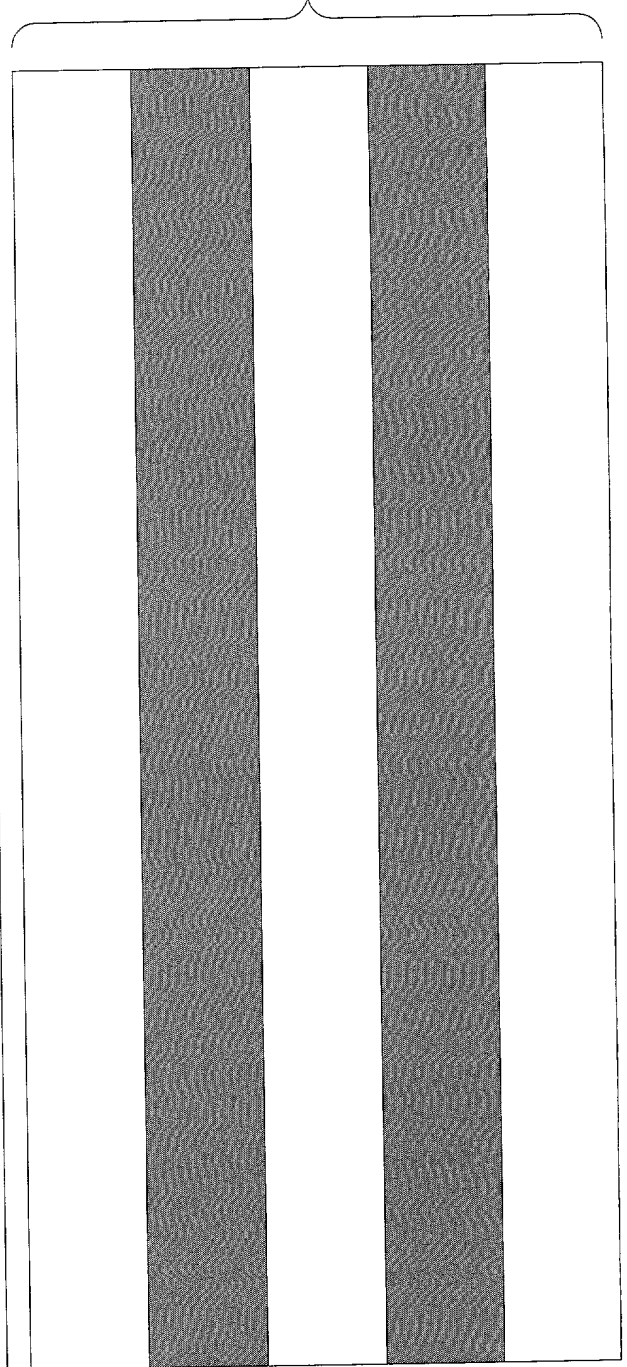


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2600

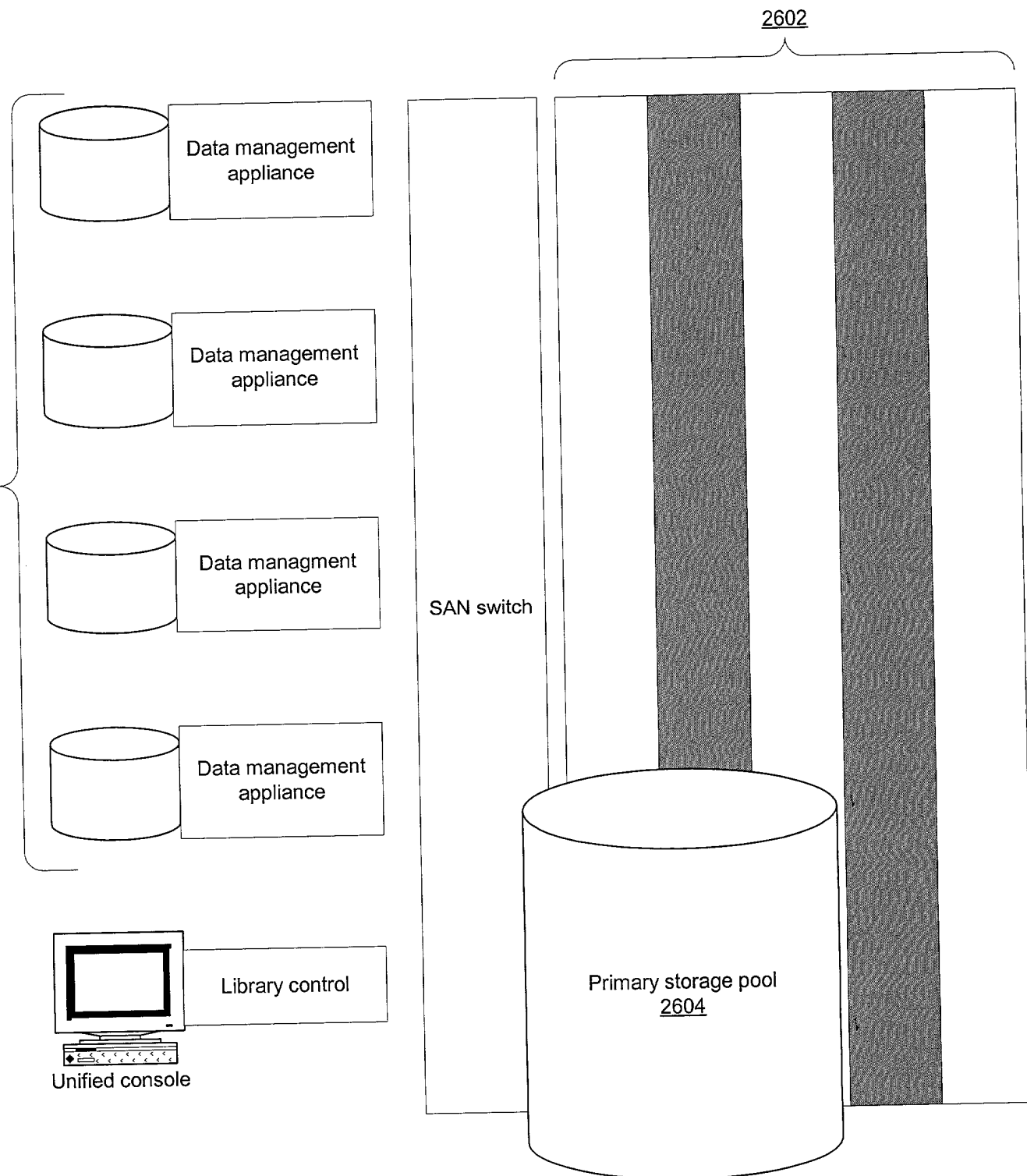


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